CLAIMS

1. A multi-chassis broadcast router (100), comprising:

a first chassis (102c) in which a first routing engine (140) and at least one clock-demanding component (136-1 through 136-N, 138-1 through 138-M) reside;

a second chassis (104c) in which a second routing engine and at least one clock-demanding component (142-1 through 142-N, 144-1 through 144-M) reside;

a first link (110) coupling an input side of said first routing engine (140) residing in said first chassis (102c) and an input side of said second routing engine residing in said second chassis (104c); and

a master clock (134) residing in said first chassis (102c), said master clock (134) coupled to said at least one clock-demanding component (136-1 through 136-N, 138-1 through 138-M) residing in said first chassis (102c) and to said at least one clock-demanding component (142-1 through 142-N, 144-1 through 144-M) residing in said second chassis (104c) via said first link (110), said master clock (134) supplying said at least one clock-demanding component (136-1 through 136-N, 138-1 through 138-M) residing in said first chassis (102c) and said at least one clock-demanding component (142-1 through 142-N, 144-1 through 144-M) residing in said second chassis (104c) with a common clock signal.

2. The apparatus of claim 1, and further comprising:

a first router matrix card (102a) supportably mounted by said first chassis (102c), said first routing engine (140) and said master clock (134) residing on said first router matrix card (102a); and

wherein said at least one clock demanding component (136-1 through 136-N, 138-1 through 138-M) further comprises at least one input card (136-1 through 136-N) and at least one output card (138-1 through 138-M).

3. The apparatus of claim 1, and further comprising:

a third chassis (106c) in which a third routing engine and at least one clock-demanding component reside;

a second link (112) coupling said input side of said first routing engine (140) residing in said first chassis (102c) and an input side of said third routing engine residing in said third chassis (106c), said master clock (134) residing in said first chassis (102c) coupled to said at

least one clock-demanding component residing in said third chassis (106c) via said second link (112);

wherein said master clock (134) residing in said first chassis (102c) supplies said at least one clock-demanding component residing in said third chassis (106c) with said common clock signal through.

4. The apparatus of claim 3, and further comprising:

a third link (116) coupling said input side of said second routing engine residing in said second chassis (104c) and said input side of said third routing engine residing in said third chassis (106c);

wherein said first routing engine (140) residing in said first chassis (102c), said second routing engine residing in said second chassis (104c) and said third routing engine residing in said third chassis (106c) are arranged in a fully connected topology.

5. The apparatus of claim 4, wherein a redundant routing engine (150) resides in each one of said first, second and third chassis (102c, 104c and 106c).

6. The apparatus of claim 5, and further comprising:

a fourth link (122) coupling an input side of said redundant routing engine residing in said first chassis (102c) to an input side of said redundant routing engine (150) residing in said second chassis (104c);

a fifth link (124) coupling said input side of said redundant routing engine residing in said first chassis (102c) to an input side of said redundant routing engine residing in said third chassis (106c); and

a sixth link (128) coupling said input side of said redundant routing engine (150) residing in said second chassis (104c) to said input side of said redundant routing engine residing in said third chassis (106c);

wherein said redundant routing engine residing in said first chassis (102c), said redundant routing engine (150) residing in said second chassis (104c) and said redundant routing engine residing in said third chassis (106c) are arranged in a second fully connected topology.

7. A multi-chassis broadcast router (100), comprising:

a first chassis (102c), said first chassis (102c) supportably mounting a first router matrix card (102a), a redundant router matrix card (102b), at least one clock-demanding input card (136-1 through 136-N) and at least one clock-demanding output card (138-1 through 138-M);

a second chassis (104c), said first chassis (104c) supportably mounting a first router matrix card (104a), a redundant router matrix card (104b), at least one clock-demanding input card (142-1 through 142-N) and at least one clock-demanding output card (144-1 through 144-M);

a first master clock (134) residing on said first router matrix card (102a) supportably mounted within said first chassis (102c), said first master clock (134) coupled to said at least one clock-demanding input card (136-1 through 136-N) and said at least one clock-demanding output card (138-1 through 138-M) supportably mounted by said first chassis (102c) and to said at least one clock-demanding input card (142-1 through 142-N) and said at least one clock-demanding output card (144-1 through 144-M) supportably mounted by said second chassis (104c), said first master clock (134) supplying said at least one clock-demanding input card (136-1 through 136-N) and said at least one clock-demanding output card (138-1 through 138-M) supportably mounted by said first chassis (102c) and said at least one clock-demanding input card (142-1 through 142-N) and said at least one clock-demanding output card (144-1 through 144-M) supportably mounted by said second chassis (104c) with a common clock signal;

a second master clock (154) residing on said redundant router matrix card (104b) supportably mounted within said second chassis (104c), said second master clock (154) coupled to said at least one clock-demanding input card (136-1 through 136-N) and said at least one clock-demanding output card (138-1 through 138-M) supportably mounted by said first chassis (102c) and to said at least one clock-demanding input card (142-1 through 142-N) and said at least one clock-demanding output card (144-1 through 144-M) supportably mounted by said second chassis (104c), said second master clock (154) supplying said at least one clock-demanding input card (136-1 through 136-N) and said at least one clock-demanding output card (138-1 through 138-M) supportably mounted by said first chassis (102c) and said at least one clock-demanding input card (142-1 through 142-N) and said at least one clock-

demanding output card (144-1 through 144-M) supportably mounted by said second chassis (104c) with a redundant common clock signal; and

control logic (148, 156) coupled to said first master clock (134) and said second master clock (154), said control logic (148, 156) determining whether said first master clock (134) should issue said common clock signal or whether said second master clock (154) should issue said redundant common clock signal.

8. The apparatus of claim 7, wherein said control logic (148, 156) has a first input coupled to said first router matrix card (102a) supportably mounted by said first chassis (102c) and a second input coupled to said redundant router matrix (104b) supportably mounted by said second chassis (104c), said control logic (148, 156) determining, based upon a first signal received via said first input and a second signal received via said second input whether said first master clock (134) should issue said common clock signal or whether said second master clock (154) should issue said redundant common clock signal.

9. The apparatus of claim 8, wherein:

a first routing engine (140) and a first transmission expansion port (146) reside on said first router matrix card (102a) supportably mounted by said first chassis (102c); and wherein:

a second routing engine (150) and a second transmission expansion port (152) reside on said redundant router matrix card (104b) supportably mounted by said second chassis (104c).

10. The apparatus of claim 9, wherein:

said first input to said control logic (148, 156) is coupled to said first routing engine (140) residing on said router matrix card (102a) supportably mounted by said first chassis (102c) and said second input to said control logic (148, 156) is coupled to said second routing engine (150) residing on said redundant router matrix card (104b) supportably mounted by said second chassis (104c); and wherein

said control logic (148, 156) has a third input coupled to said transmission expansion port (146) residing on said router matrix card (102a) supportably mounted by said first chassis (102c) and a fourth input coupled to said second transmission expansion port (152) residing on said redundant router matrix card (104b) supportably mounted by said second chassis (104c)

said control logic (148, 156) determining, based upon said first signal received via said first input, said second signal received via said second input, a third signal received via said

third input and a fourth signal received via said fourth input, whether said first master clock (134) should issue said common clock signal or said second master clock (154) should issue said redundant common clock signal.

11. The apparatus of claim 10, wherein said control logic (148, 156) further comprises:

a first state machine (148) residing on said first router matrix card (102a) supportably mounted by said first chassis (102c);

a second state machine (156) residing on said redundant router matrix card (104b) supportably mounted by said second chassis (104c);

said first state machine (148) determining, based upon said first signal received via said first input, said second signal received via said second input, said third signal received via said third input and said fourth signal received via said fourth input, whether said first master clock (134) should issue said common clock signal; and

said second state machine (156) determining, based upon said first signal received via said first input, said second signal received via said second input, said third signal received via said third input and said fourth signal received via said fourth input, whether said second master clock (154) should issue said redundant common clock signal;

wherein only one of said common clock signal and said redundant common clock signal can be issued at one time.